Amendments to the Specification:

Please replace the TITLE with the following rewritten TITLE:

--REGISTER CONTROLLED DELAY LOCKED LOOP HAVING AN ACCELERATION MODE--

Please replace the paragraph at page 1, lines 6-8 with the following rewritten paragraph:

--The present ~~invention~~ disclosure relates to a semiconductor circuit technique[[;]] and, more particularly, to a ~~resister~~ register controlled delay locked loop DLL having an acceleration mode.--

Please replace the paragraph beginning at page 21, line 20 and ending at page 22, line 15 with the following rewritten paragraph:

--In the present invention, the DLL should perceive what time the acceleration mode is terminated in a bad condition that a rising edge occurs at every 1 tCK, because of usage of a free-running clock signal instead of a divided clock signal. The acceleration mode should not be executed if the delay value N x unit_delay of the delay logic 63 is larger than a half period of ~~a maximum frequency `tCK,min`~~ a maximum frequency signal as reference value. However, the acceleration mode is executed because the acceleration mode termination signal accel_end is 0. Namely, a maloperation ~~is occurred~~ occurs when the rising edge of the output fb_dm of the delay model 59 [[is]] corresponds to a period that the non-delayed input clock signal rclk is in a logical high state and the rising edge of the output fbclk_dly of the delay logic 63 [[is]] corresponds to a period that the non-delayed input clock signal rclk is in a logical low[[.]] state. The reason for this maloperation is because the two phase comparators 60 and 64 ~~can not~~ cannot perceive whether ~~or not~~ the rising edge of the fb_dm and that of the fbclk_dly ~~are occurred~~ occur in the same period that the second non-delayed input clock signal rclk is in a logical high[[.]] state. Thus, an approved range of N is determined to be lower than a half period (1/2 x tCK,min) of the maximum operating frequency signal, which is the reference for the delay value N x unit_delay of the delay logic 63.--

Please replace the paragraph at page 22 , lines 16-23 with the following rewritten paragraph:

--For instance, assuming that the maximum operating frequency of the operating signal is 333 MHz, i.e., tCK,min=3 ns, and the delay value of the unit delay cell UDC is 150ps, the following equation 1 is formulated. ½ x 3 ns>N x 150 ps (Eq. 1) This equation indicates that N is ~~fewer~~ less than 10.--